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a number of bumps formed respectively in said through-holes of said wiring substrate in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

an external bump pad for said bump electrically connected to said at least two chip electrodes.

22. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes of said wiring substrate in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

an external bump pad electrically connected to said at least two chip electrodes.

23. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said

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semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

an external bump pad electrically connected to said at least two chip electrodes.

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27. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring of said wiring substrate respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected to said at least two chip electrodes.

28. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of working formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of

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said wiring substrate, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

an external bump pad electrically to said at least two chip electrodes.

29. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

an external bump pad electrically connected to said at least two chip electrodes.

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33. (Thrice Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said

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semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

an external bump pad electrically connected to said at least two chip electrodes.

34. (Thrice Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring of said TAB tape is bent at at least one position;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

an external bump pad electrically connected to said at least two chip electrodes.

35. (Thrice Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

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a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring of said TAB tape has an end width larger than an inter-electrode distance between said chip electrodes;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

an external bump pad electrically connected to said at least two chip electrodes.

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39. (Thrice Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring of said TAB tape respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

an external bump pad electrically connected to said at least two chip electrodes.

40. (Thrice Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

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a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring of said TAB tape respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

an external bump pad electrically connected to said at least two chip electrodes.

41. (Thrice Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring of said TAB tape respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

an external bump pad electrically connected to said at least two chip electrodes.

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### REMARKS

Independent claims 21-23, 27-29, 33-35 and 39-41 have been amended to better define the instant invention over the prior art. More particularly, each of the pending independent